

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan.

PUBLICATION NUMBER : 2000243953
PUBLICATION DATE : 08-09-00

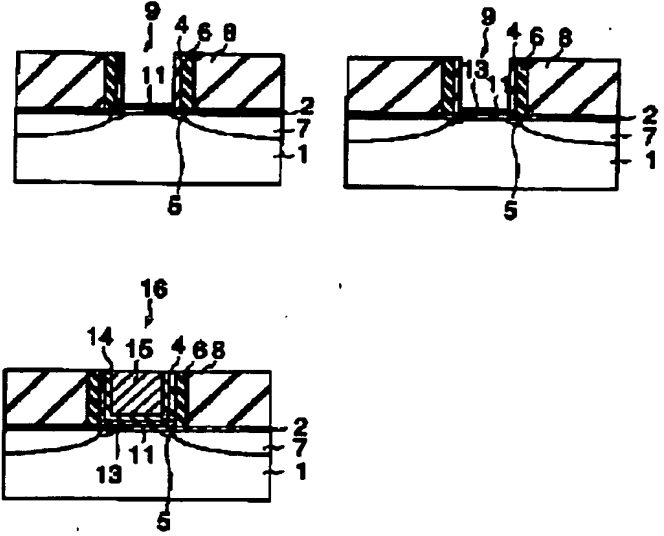
APPLICATION DATE : 22-02-99
APPLICATION NUMBER : 11042736

APPLICANT : TOSHIBA CORP;

INVENTOR : INUMIYA SEIJI;

INT.CL. : H01L 29/78 H01L 21/283

TITLE : SEMICONDUCTOR DEVICE AND
MANUFACTURE THEREOF



ABSTRACT : PROBLEM TO BE SOLVED: To realize high operational speed of an element by suppressing a wiring resistance of a gate electrode.

SOLUTION: As shown in (g), immediately after an exposed surface of a silicon substrate 1 at a bottom surface of an opening 9 is made hydrophobic, a Ta₂O₅ film 11 is deposited to have a thickness of about 5 nm on the substrate surface by a CVD method. In this case, the Ta₂O₅ film 11 is formed only on the substrate 1 at the bottom surface and not formed on a side wall of the opening 9 or on a silicon oxide film 8. Then as shown in (h), the laminate is subjected to an annealing process in an atmosphere containing, e.g. oxygen activating species of 300°C, to form a 1 nm thick silicon oxide film interfacial layer 13 on the interface between the silicon surface and film 11. Thereafter, a for example, a 10 nm thick titanium nitride film 14 and a 300 nm thick aluminum film 15 are deposited, the entire surface of the laminate is flattened by a CMP method to form a buried gate electrode 16. As a result, a transistor structure is formed as shown in (i).

COPYRIGHT: (C)2000,JPO